2023-2024 spring capstone final report: <https://docs.google.com/document/d/1QNvqZRcIlr5oz7clWzOwtHOtSd97eKo5BvxzaM-GsSM/edit>

Github wiki: <https://github.com/Epsilon391/High-Frequency-Sampling-for-Circuit-Analysis>

STM32F103C8T6

10/09/2024:

* Starting BOM, starting with materials used in current setup
  + BOM in separate google sheets

10/10/2024:

* Signed into altium and got student license set up
* Started going through altium education courses
  + Completed unit 1: intro to PCB design
* Complete Altium Design Walkthrough:
  + <https://www.altium.com/documentation/altium-designer/tutorial-complete-design-walkthrough>
* Potential rpi3 hat template:
  + <https://github.com/NilsMinor/Raspberry-Pi-3-Altium-Template>
* \*Q\*: Oh my gosh how am i going to do the uart to usb?
  + Figure out which rpi3 pins correlate to usb and connect the uart to that?
  + Have external plug from hat to usb? That sounds so stupid
* STM32F103C8T6 (not blue pill) footprint and symbol:
  + <https://www.snapeda.com/parts/STM32F103C8T6/STMicroelectronics/view-part/>
* Blue Pill library:
  + <https://drive.google.com/drive/folders/1h2A7z9TJHi94DTVskRtiVFdMy21IkLaa>
    - Youtube that this came from: <https://www.youtube.com/watch?v=6_43WsJML8A>
  + Added to OSGC drive in research/blue\ pill
* Working through altium unit 2
  + Ended at “Finding Components in Altium Designer”

10/14/2024:

* Unit 2.3: “It’s important to note that you won’t have to create every new component that appears in your design. However, there are times where components can’t be found in the Manufacturer Part Search panel or Components panel, and so you’ll need to create the symbols and footprints yourself. To see how to do this, read the Appendix to this course to see a short guide on creating CAD data for your components.”
* Finished unit 2 of altium education

10/15/2024:

* Started unit 3 of altium education
  + ‘Cntl + q’ for changing units from imperial to metric
* QUESTION(S):
  + How will I make sure I get enough power to the chips on board?
    - Current amp requires 9 V, so will I step up the voltage from the rpi?
    - Blue Pill requires 3.3 V (has 3.3 V regulator so slightly more is okay I think), also step up rpi voltage?
* Just about finished unit 3
  + Need to finish practice component layout and quiz

10/17/2024:

* Finished unit 3
* Starting unit 4
* ‘Cntrl + shift’ + scroll mouse wheel to place a via and continue scrolling to choose which layer to route to

10/20/2024:

* I didn’t finish unit 4 but i think i went through all of the stuff i was worried about for now
  + May come back to it later
* I think i shall use this rpi3 hat board design:
  + <https://github.com/NilsMinor/Raspberry-Pi-3-Altium-Template>
  + I’ll likely have to add more layers, I’m sure that’s possible
* Looking into this:
  + Blue Pill library:
    - <https://drive.google.com/drive/folders/1h2A7z9TJHi94DTVskRtiVFdMy21IkLaa>
      * Youtube that this came from: <https://www.youtube.com/watch?v=6_43WsJML8A>
  + Having trouble with this, will revisit
* Started making schematics for easy stuff like highpass filter
* Jlcpcb parts: <https://jlcpcb.com/parts>
* Somehow made capacitor footprint? Made one for a cap that is available on jlcpcb and included it in BOM
  + Used the british expression measurements from this datasheet: <https://www.lcsc.com/datasheet/lcsc_datasheet_2304140030_FH--Guangdong-Fenghua-Advanced-Tech-0603B203K500NT_C1602.pdf>
* Made a resistor footprint too :)
* Drew the schematic of the high-pass filter woot woot
* Next step: amplifier
  + Look for library/footprint, else make my own :,)

10/22/2024:

* AD620 IA:
  + <https://github.com/butterwick/AltiumLibrary/blob/master/Libraries/Analog%20Devices/AD%20Instrumentation%20Amplifier.IntLib>
  + <https://www.digikey.gr/en/models/617755>
* In Altium Designer, a component can have multiple footprints to meet the IPC requirements for different density levels:
  + L: Least or minimum copper
  + M: Most or maximum copper
  + N: Nominal or median copper
* Got all the big ICs into altium for the AD620 IA and updated BOM

10/27/2024:

* Following youtube video to create STM32!
  + Blue Pill library:
    - <https://drive.google.com/drive/folders/1h2A7z9TJHi94DTVskRtiVFdMy21IkLaa>
      * Youtube that this came from: <https://www.youtube.com/watch?v=6_43WsJML8A>
* Tools -> component placement -> reposition selected components
* Did stm32 bluepill pcb layout by following tutorial

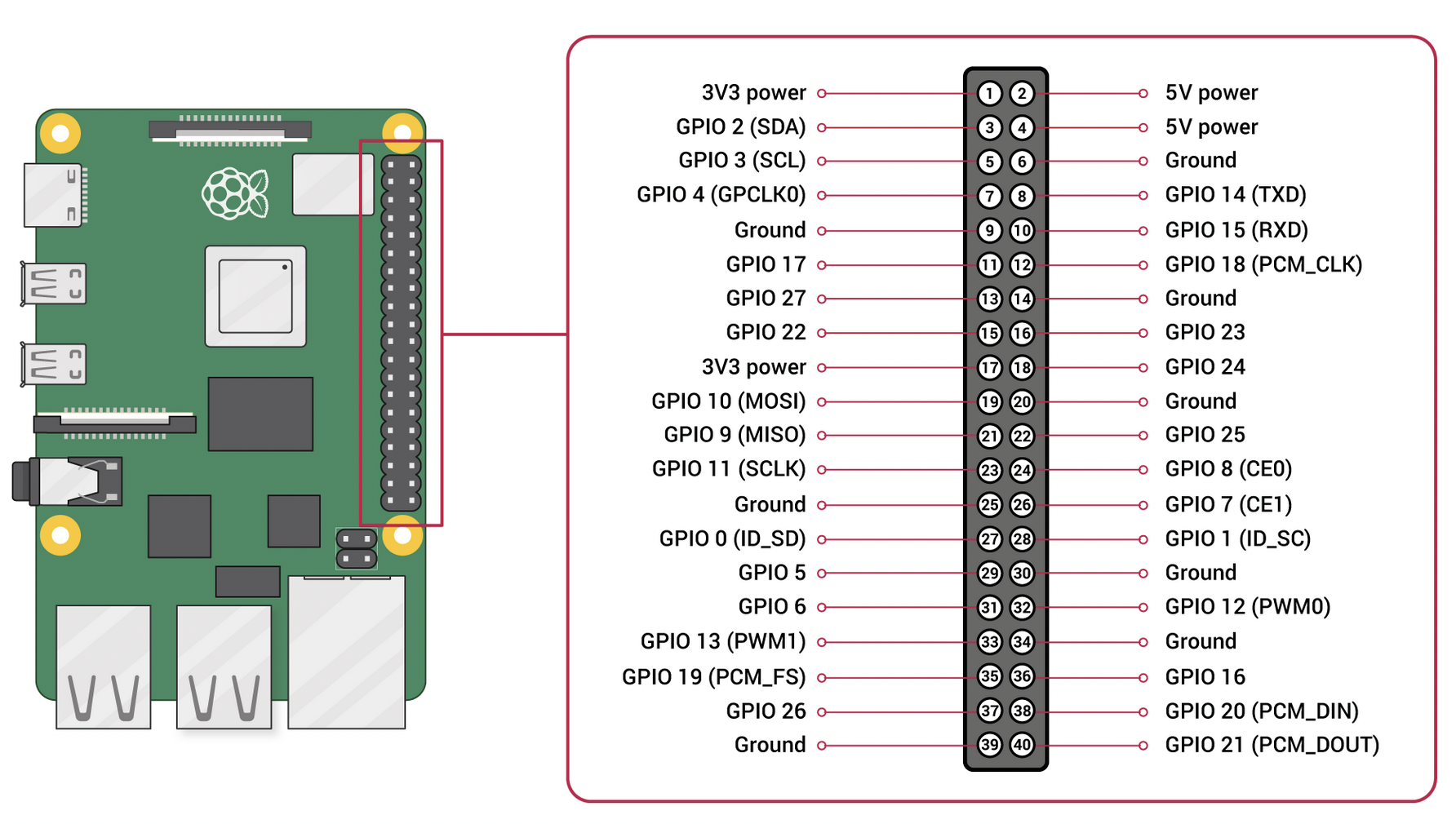
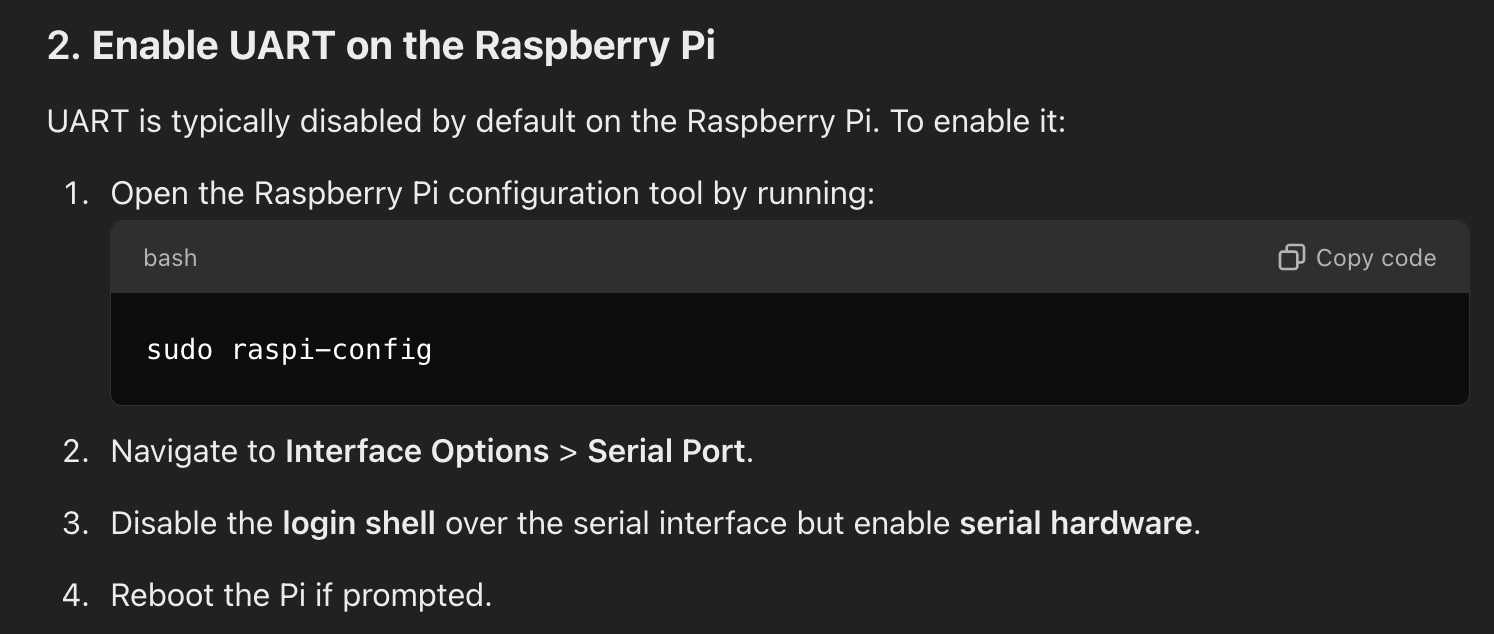
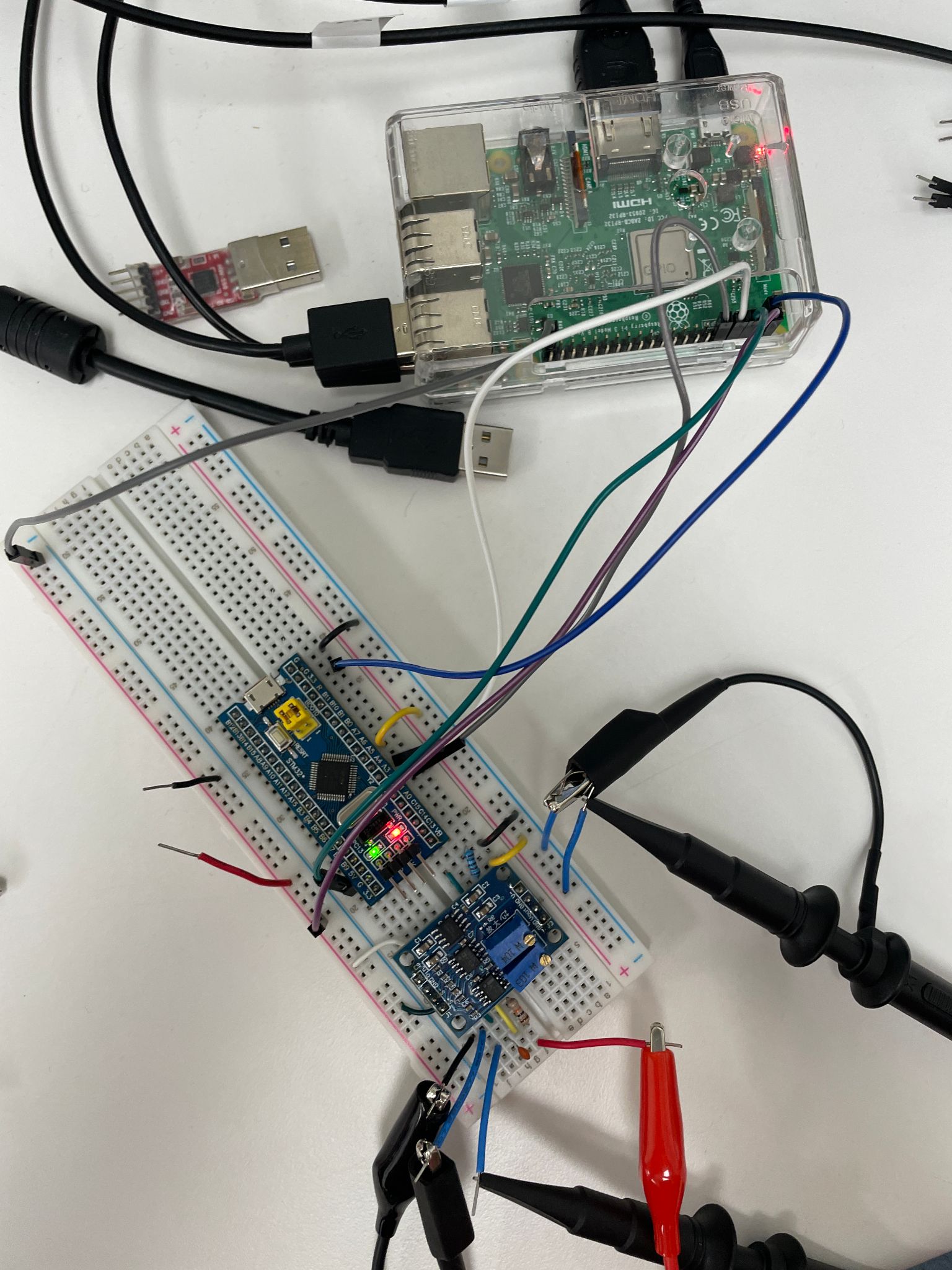
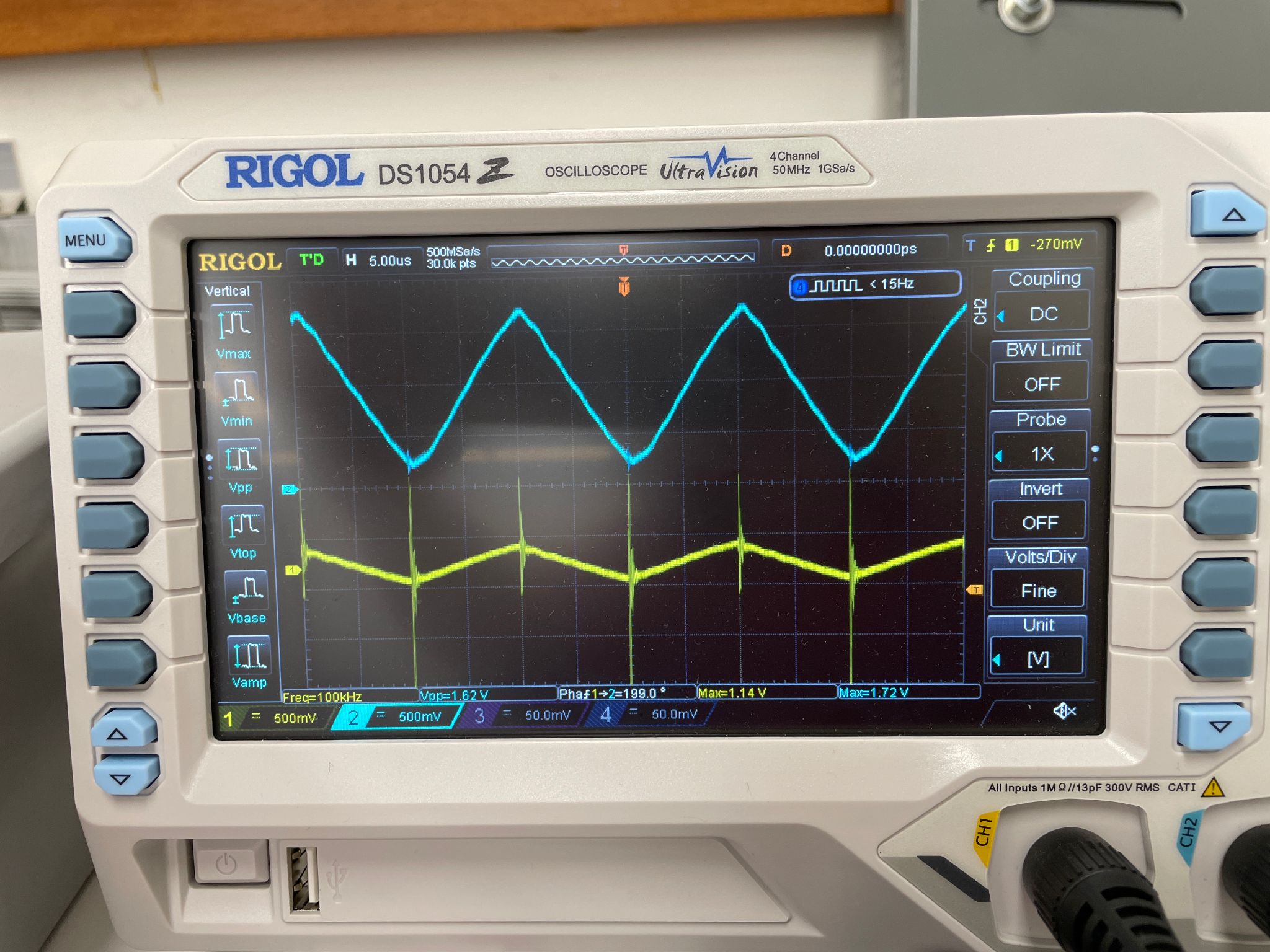
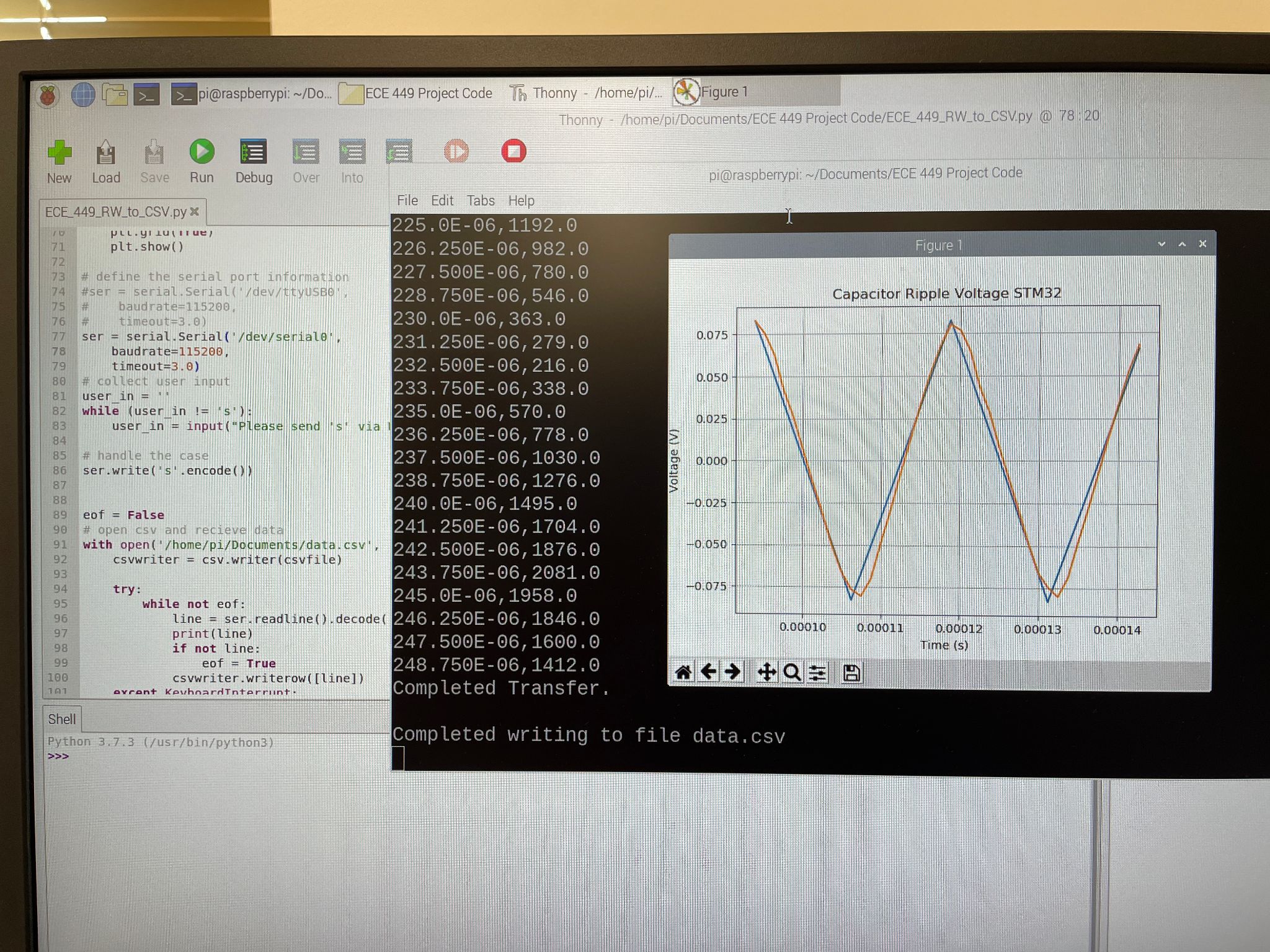
10/29/2024:

* Starting to stress about how much time i have left
* Things i need to do:
  + Finish up amp schematic
    - Verify power levels are fine for all components
    - Fix nets and stuff
    - Connect to highpass filter
    - ~~Add boost converter~~
    - Add pots
  + Get headers for stm32 bluepill to plug into shield
    - Measure stm32 bluepill
  + Figure out how to connect everything to rpi3 through shield
    - Oh shoot i need to figure out uart to usb stuff
      * There are direct UART0 TX/RX pins, so connect to those
    - Rpi has 3.3V pins, so use those for STM32
    - ~~Rpi also has 5V pins, so step those up to 9V for amp~~
      * Or just use 5V for amp, as tested below
* Ask dr scott schematic questions
  + Marked on amp schematic photos in drive
* Test to see if amp works with 5V input so i can pull it from rpi instead of using boost converter
  + It does work with 5V input
    - Is it fine if i use the 5V from the rPi for the amp then? This would eliminate the need for the boost converter
  + Documented photos and a video of how changing the input voltage affects the amplified signal (in google drive)
  + I’m assuming changing the input voltage changes the max amount of amplification you can do of the signal
* Test to see if i can pull 3.3V and 5V from rPi header pins and send into amp and bluepill
  + Need to grab female to make wires for that, or at least female to female

10/30/2024:

* C7 close to U2, C2,3,4,5 close to U1, add 100nF cap from U3A pin 8 to ground (decouping)
* Place no connection (x) on lines that are not connected
* Follow second schematic and add 1x100nF cap from pin 4 to ground and another from pin 8 to ground
* Altium: place -> directives -> no connections

10/31/2024:

* Fixed as many schematic design errors as I could and left that once I couldn’t and that I thought wouldn’t affect the circuit
* Found trimpots for schematic and saved footprints already created
* Replaced some schematic parts with altium generated footprints etc
* Schematic validation report in google sheets
* Tested using rpi3 GPIO pins to power amp and bluepill as well as doing uart comms
  + Rpi3 5V → amp v\_in ✅
  + Rpi3 GND → amp GND ✅
  + Rpi3 3.3V → bluepill 3.3V ✅
  + Rpi3 TX → bluepill RX ✅
  + Rpi3 RX → bluepill TX ✅
  + Rpi3 GND → bluepill GND ✅
* Had to adjust rpi3 config settings and adjust python script to execute uart comms using GPIO pins instead of UART to USB
  + Changed wiring from bluepill to rpi3 (used to go to USB connector, now goes to GPIO pins 6, 8, 10)
    - ****
  + ****
  + **ECE\_449\_RW\_to\_CSV.py**
    - ‘/dev/ttyUSB0’ → ‘/dev/serial0’
* Success!
  + 
  + 
  + 

11/01/2024:

* Use through-hole trimpots
* Add probe things for connecting Vload
  + Wire to board, wire to PCB, terminal block
  + Use the ones with screws
  + Can add test points additionally
* Fixed up schematics real good
* Got footprints for plugin trimpots
* Got footprint for bluepill headers and fixed that schematic
* Connected all of the schematics together!
* Added test points
  + Was generous with them, maybe reduce number of them
* Need to get terminal thing still
* Should fr test that all components are okay power-wise

11/04/2024:

* Review that one IC that was expensive, prob dont need B version
* 4 layer board
  + Important signals closer to ground
  + Signal, power (5/3.3V), GND, signal
* Only use through vias
  + No blind or buried vias
  + 5V, 3.3V, GND through vias

11/05/2024:

* Checking power going through components
  + R9 concern
    - 10 ohm with 5V going through it -> P = 2.5 W
    - Rated for 0.1W
    - 1% tolerance
  + Everything else seems okay
  + Caps are all rated for 6.3 V or higher
* What would be the best tolerance?
  + Is 1%, 10%, 20% okay or should I be consistent between components?
  + What is “high” tolerance? 20%?
* Got terminal block in altium
* Started layout!!

11/06/2024:

* option to solve power rating problem:
  + Use 1 larger 2512 surface mount resistor
    - Look for cheapest option
    - Needs to still equal 10 ohm
* Change all caps to be 25V rating **at least**
  + No price difference between 25V and 50V 0.1 uF
  + Try for 50V rated, but 25V would be fine
  + Change all caps to 0805
* Still need to change that one B quality component
* Murata or yageo for caps, or TDK, vishay, wurth
* Tolerance, lowest percentage possible
  + 1% is good

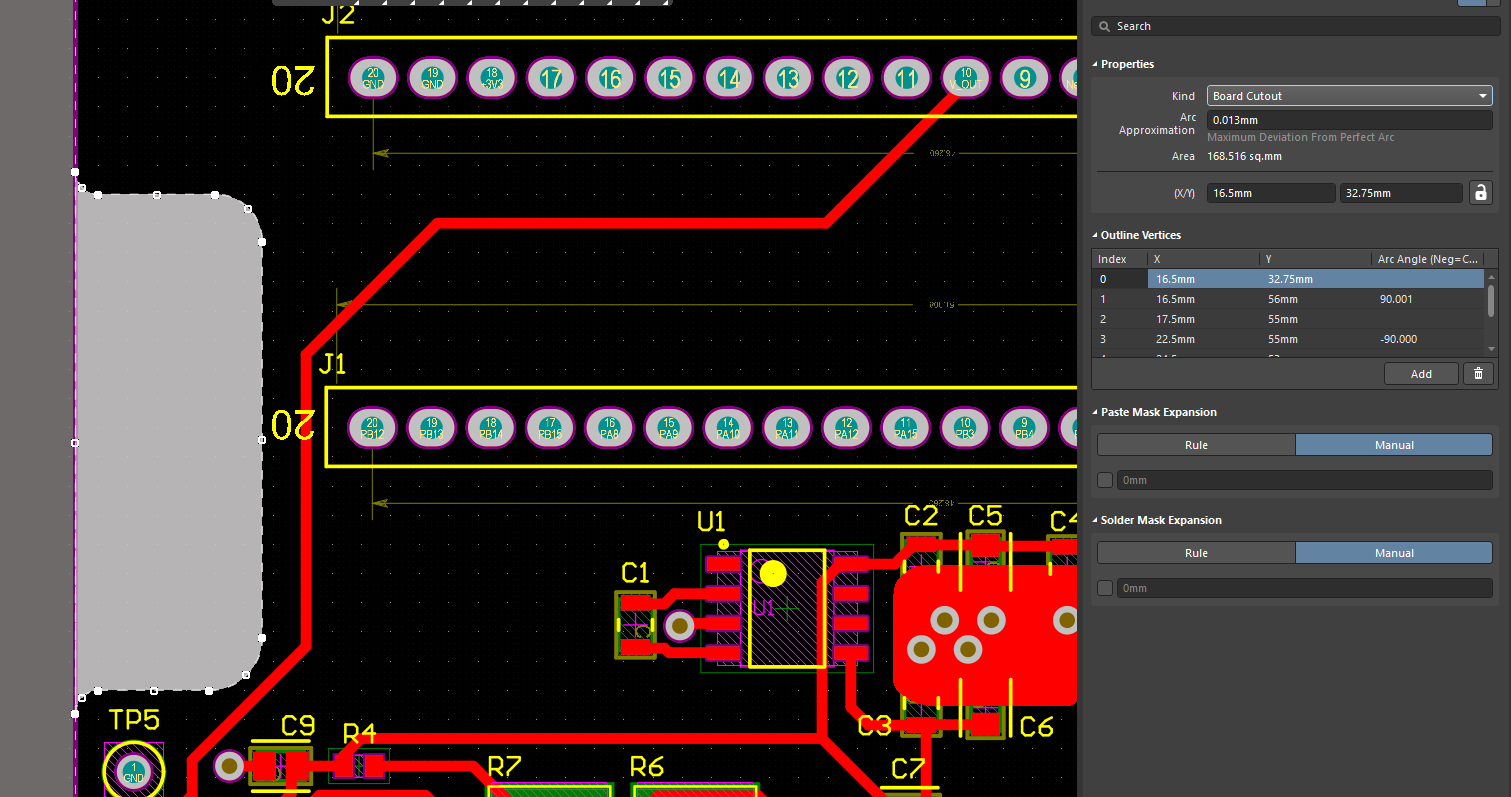
11/07/2024:

* Replaced AD620BRZ with AD620ARZ
* Replaced all caps with 0805 50V equivalents
  + 20 nF and 100 nF have 5% tolerance
  + 10 uF has 10% tolerance - is this an issue?
* Still deciding which 10 Ohm resistor to use
  + Found some 2512 options
    - 2W and 5% tolerance from trustworthy companies
    - 1W and 1% tolerance from trustworthy companies
    - 2W and 1% tolerance but potentially sus company
  + Found a 2W 1% tolerance from Yageo so going with that
* review IC footprint
* Traces: don't go below 20 mils - go bigger if you can
* Dr Scott uses a lot of polygons

11/12/2024:

* ~~Run Vout on the top layer~~
* ~~Expand 5V polygon to take over left-most 3V3 stuff~~
  + ~~When breaking 3V3 connection to pin, reroute on another layer, prob bottom layer~~
* ~~Design clearance: 8 mils between trace and pad and see if i can make it work~~
  + ~~6 mils minimum~~
* Mine is set to .254 mm
* ~~Traces~~
  + ~~Can get away with 10 mils for signal traces if needed~~
  + ~~Keep power traces 20 mils~~
* ~~Add ground vias next to each capacitor C2-8~~
* ~~Move trace by bluepill bottom right ground pin to add second connection to gnd~~
* ~~Remove thermal reliefs for ground and power vias (will affect all vias)~~
  + ~~In design rules~~
  + ~~plane/polygon connect~~
  + ~~“Direct connect” instead of thermal relief~~
* ~~Also add via next to C9, C1~~
* ~~Dont want sharp edges with polygons~~
  + ~~Hit shift space or something like that to round edges~~
  + ~~Set grid to 50 mils for easier and cleaner time~~
* Gonna want to make a mechanical layer for manufacturer
* ~~Use grid to snap components into place, use bigger grid to snap to place~~
* ~~Run keepout layer through bluepill pins that arent being used~~
  + ~~Looks like large trace going through pins~~
* ~~On bluepill headers and rpi headers~~
  + ~~Make pads bigger, increase diameter, make shape 2 mm, twice hole size~~
  + ~~Need 10 mils of space between pads (could get away with 0.6)~~
* ~~Can grab component to move it and jump to specific coordinate (some keybind)~~
  + ~~Maybe “J+C”~~

11/14/2024:

* When i made the pads bigger, they got ovular. Is this normal?
  + Did hole size 1mm, diameter 2mm
* Review power layer with dr scott
  + Did keepout traces and then removed them bc they made design errors but kept polygon pour from then they were were
* Rounded all polygon corners
* is top layer ground polygon/vias improved?
* Is layer stackup okay?
* For the BOM that I’ll submit when ordering the PCB, is the one I made good or do i use the one altium made and then alter it?
* Does this count as a cutout or do i need to somehow have it outlined in purple too?
  + 

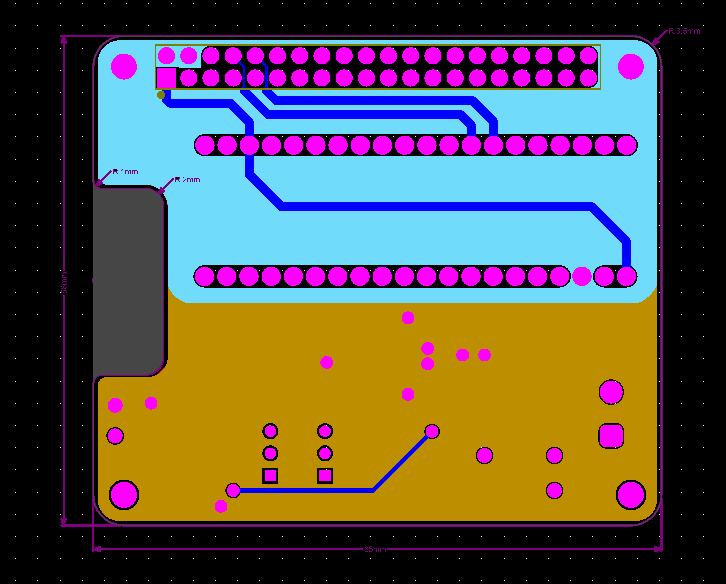
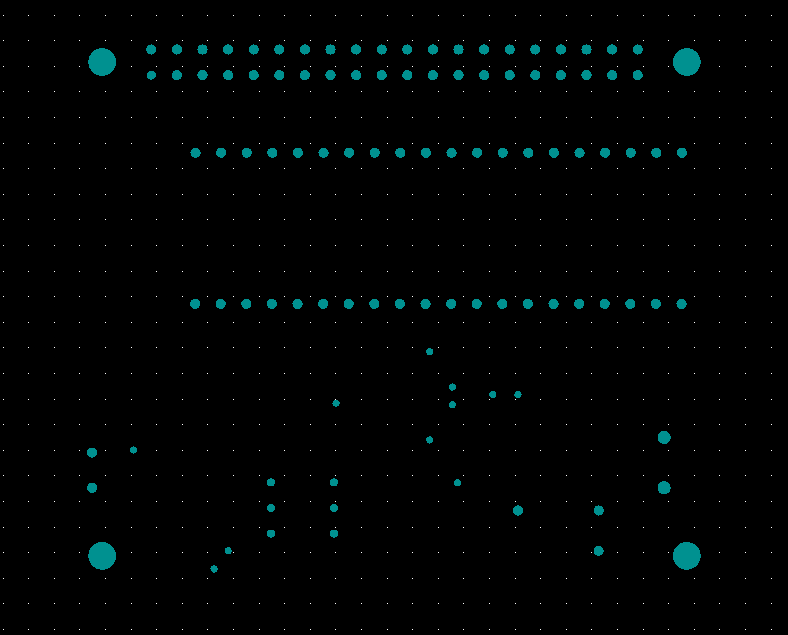
11/19/2024:

* Move C5 and C6 90 degrees and placed super close to pins
* Move trace 8 under U1 to the center and make trace a big polygon connecting all the stuff
* Make 5V polygon bigger and try to go around the standoff
* ~~Make standoffs ground vias~~
* Do not populate (DNP) for parts i don’t want JLC to put on there
* Add cutout to mechanical outline?
  + Either add to M2 or make my own
* Email jlc and ask if theyd be able to make the cutout with the altium stuff as is
  + Outline and schematic
* Added mechanical outline for cutout
  + Add note to mechanical outline layer on gerber file for cutout
    - Also include dimensions
* Had to make bottom-side traces between rpi header 10 mil and those pads 1.75mm with 1mm hole
  + (is this okay?)
  + Otherwise i can go around the outside of the header
* Routed 1 3V trace on top side and left the others on the bottom side
* Went kind of crazy with the polygons
  + (is this okay?)
  + Should i add more? lol
* Adjusted standoff holes, did not make them ground vias

11/20/2024:

* Added mechanical outline for cutout
  + Add note to mechanical outline layer on gerber file for cutout
    - Also include dimensions
* Add keepouts on power layer thing
* Make 3V3 traces bigger
  + 50 mils instead of 20
* Npt - non plated through-hole
  + Unplate standoff
* Label Vin/GND on board

11/21/24:

* Jlcpcb people responded about tax - relatively unhelpful
* Fixed up rest of board
  + Added dimensions
* Terminal block wasn’t available on jlcpcb so i’ll order it from digikey and solder it on myself
  + Made the pads bigger
* Make jlcpcb and digikey carts
  + <https://jlcpcb.com/user-center/smtPrivateLibrary/partsCart/>
  + <https://www.digikey.com/ordering/shoppingcart?lang=en>
* Followed this to make gerber files: <https://jlcpcb.com/help/article/How-to-export-Altium-PCB-to-gerber-files>
  + 
  + 
  + Not sure if this is correct
* files:
  + Copper, mask, overlay for top and bottom
  + Inner planes
  + Mechanical layer
  + Drill file
  + 10 total

—

Altium

* Filename Structure Layout
* xxx.gtl Top Copper Layer
* xxx.gbl Bottom Copper Layer
* xxx.g1 Inner Copper Layer
* xxx.gm3 Board Mechanical Layer
* xxx.gko Board Outline
* xxx.gto Top Silkscreen
* xxx.gbo Bottom Silkscreen
* xxx.gts Top Soldermask
* xxx.gbs Bottom Soldermask
* xxx.gtp Top Solderpaste
* xxx.gbp Bottom Solderpaste
* xxx.txt Drill Layer
* Got all gerber files
* Cutout not shown on uploaded file but is shown in board layout
* <https://jlcpcb.com/help/article/Instructions-for-ordering>